

44. The apparatus according to claim 43, wherein the switching element is a CMOS transistor.

45. The apparatus according to claim 43, wherein the D/A converter is capable of inputting one bit more than the bit number of the picture data bits, and the signal-polarity inverting signal is inputted to the most significant bit of the D/A converter.

A3 46. The apparatus according to claim 43, wherein said apparatus has a booster circuit for boosting the output of the D/A converter.

47. The apparatus according to claim 43, wherein the booster circuit comprises a clamp type amplifier.

48. The apparatus according to claim 43, wherein the D/A converter provides analog signals by selecting one point of a resistance element connected in series by decoding digital signals of more significant bit and less significant bit.--

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REMARKS

Claims 1 and 18 have been amended in order to recite

the present invention with the specificity required by statute and Claims 5 and 22 have been amended for better conformity with accepted U.S. practice. Additionally, new Claims 38-48 are presented in order to more specifically recite various preferred embodiments of the present invention. Finally, claims 6 and 23 are amended as superfluous, and the title has been amended in order to more clearly relate to the claimed invention. Accordingly, no new matter has been added.

The claims stand rejected under 35 U.S.C. §102(e) as anticipated by Lewis U.S. Patent No. 5,589,847 (claims 1-12, 15-16, 18-29, 32-33 and 35) or under 35 U.S.C. §103 as obvious over Lewis in view of Misawa U.S. Patent No. 5,250,931 (claims 13-14, 17, 30-31, 34 and 36-37). The Examiner's bases for the rejection is set forth in detail from pages 2-11 of the Office Action.

This rejection is respectfully traversed, in particular, based on the foregoing amendment and the following remarks.

Specifically, in support of the rejection, the Examiner states that

In regards to claim 6, Lewis discloses inputting signal-polarity signals, and inverting the polarity of output signals [see Figure 5, Column 7, Lines 25-65].

Respectfully submitted, the Examiner's understanding in

this regard is incorrect. That is, Applicants' detailed review of Lewis shows that the cited text merely discloses a "switched capacitor circuit", which is understood by those of ordinary skill to be quite different from a polarity inversion means as recited in the present invention. Accordingly, Lewis neither discloses nor suggests the subject matter of the pending claims, which includes this salient feature.

Moreover, this deficiency is not remedied by Misawa, which has been cited as being relevant for signal decoding methodology (claims 13 and 30), diffusion layers with impurity concentrations (claim 14 and 31), etc. In particular, Misawa does not teach or suggest means for inputting signal-polarity inverting signals together with the picture data, and for inverting the polarity of an analog output of a D/A converter. Accordingly, there is no *prima facie* obviousness of the pending claims and the rejection over the prior art should be withdrawn.

In view of the above amendments and remarks, Applicants submit that all of the Examiner's concerns are now overcome and the claims are now in allowable condition. Accordingly, reconsideration and allowance of this application is earnestly solicited.

Claims 1-5, 7-22 and 24-38 remain presented for continued prosecution.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should be directed to our below listed address.

Respectfully submitted,

  
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